Paper No. 27

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

_____

Ex parte PIERRE HUON AND
RENE GLAISE

_____

Appeal No. 96-0033
Application 08/066,638[1]

_____

ON BRIEF

_____

Before THOMAS, MARTIN and LEE, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 1 to 9, which constitute all the claims in the application.

[1] Application for patent filed May 25, 1993, which is a continuation of Application 07/491,901, filed March 12, 1990, now abandoned.

Representative independent claim 1 is reproduced below:

1. A circuit for controlling data transfers between a first device (1) and a second device (2) which operate at different data rates, the first device providing data on an output bus at a first rate together with strobe signals indicating data is available to be transferred, the second device receiving data at a second rate which is the rate of clock signals provided by the second device, comprising:

at least R buffer registers (10, 12; 210) for receiving data from the first device, R being an integer number equal to T+(T-1) x (B-1), where T is a maximum number of data entities that can be provided by the first device in a period of a clock signal and B is a number of consecutive periods during which the first device can provide a maximum number of data entities,

counting means (28;222) for generating R x (R+1) distinct values in response to the strobe signals applied thereto;

decoding means coupled to the counting means, for generating signals representative of the values generated by the counting means and active loading signals used to cause the data from the first device that are available at each strobe signal to be loaded in a register selected among the buffer registers (R1 to Rr) in a fixed sequence;

gating means (16, 20, 216), coupled to the buffer registers, for selectively gating the data from the first device into the buffer registers in response to said active loading signals;

storing means (44) responsive to the strobe signals, the clock signals provided by the second device and the signals representative of the values generated by the counting means, for keeping track of those buffer registers which contain data from the first device and of the sequence in which the buffer registers were loaded; and

selection means (40, 34, 240, 234) responsive to signals outputted from said storing means and to the signals representative of the values generated by the counting means

for selectively gating the data from the buffer registers to the second device, in such a way that the data are provided to the second device in the same sequence as they were provided by the first device.

The following references are relied on by the examiner:

Meinke	4,193,123	Mar. 11, 1980
Trost	4,288,860	Sep. 8, 1981

Claims 1 to 9 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon Trost alone as to claims 1 to 5, 8 and 9, with the addition of Meinke as to claims 6 and 7.

Rather than repeat the positions of the appellants and the examiner, reference is made to the brief and the answer for the respective details thereof.

OPINION

For all the reasons well expressed by the examiner in the answer, and for the additional amplifying reasons presented here, we will sustain the prior art rejection of claims 1 to 5, 8 and 9. However, we reverse the rejection of dependent claims 6 and 7.

In addition to a detailed correspondence of the structure of representative independent claim 1 on appeal in the statement of the rejection in the answer, the examiner has addressed each of the arguments presented by appellants beginning at page 8 of the brief. We add our own views as to these arguments.

At page 9 of the brief, appellants assert that Trost does not show the claimed decoding means. Appellants' position questions the ability of the decoding means claimed to be met in the context of the position that there are no "strobe in" signals of the argued decoding means in Trost. This position is misplaced since the corresponding clock signal 41 exiting the dynamic storage means 10 in Figure 1 in Trost corresponds to the claimed strobe signal.

At the same time as recognizing at the bottom of page 8 of appellants' brief that the examiner has found correspondence in Trost for all the subject matter of the appealed claims, appellants assert at the bottom of page 9 of the brief that the examiner's identification of the various columns and portions of figures in the statement of the rejection is insufficient. The examiner's approach is conventional in setting forth the statement of the rejection and appellants' comments at the bottom of page 9 and the top of page 10 of the brief are misplaced since

they fail to consider a reasonable association of the teachings of the reference to the scope of the claims on appeal. As pointed out by the examiner at pages 8 and 9 of the answer, such a presentation belies the prosecution history of this application. In any event, appellants' further assertion that the examiner has, by this approach, not met the rationale of In re Donaldson Co., 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994), is also misplaced. The examiner's basic position asserts either corresponding structural elements or the structural equivalence of the claimed elements rejected, which approach shifts the burden to appellants to detail what portions of the specification disclosed for those claims utilizing the means-plus-function format of 35 U.S.C. § 112, paragraph six, are not in the reference. This burden appellants have not met.

Appellants' assertion at the bottom of page 10 and on top of page 11 of the brief is also misplaced in that it is immaterial to the scope and subject matter of the claims on appeal whether or not the reference requires an external clock to control the data rate transfers. The clocking control circuit 24 in Figure 1 of Trost operates in conjunction with the clocking signal provided on line 41 from the dynamic storage device 10, as well as the clock signal provided from the requestor 11 on line 40.

Furthermore, as said by the examiner at page 10 of the answer, there is nothing in appellants' claims to preclude that a first rate from a first device may be variable, as is taught in Trost, or to preclude that this rate may be externally provided to the overall device.

Appellants' positions presented between pages 11 and 13 are also non-persuasive since they appear to argue the disclosed rather than the claimed invention. As to appellants' position at page 13 of the brief, there is no claimed burst mode of the first device recited in any independent claim on appeal. There is only an implication or an inference that may be derived from the language of the register means clause that something other than a maximum number of data entities may be transferred within consecutive clock periods at other times. Even as disclosed, appellants' memory device 1 does operate in at least two speeds, a normal speed and a burst mode speed. As set forth at columns 1 and 2 of Trost, the dynamic memory of this reference embodied as element 10 contains the capability of operating at two speeds, a fast and a slow speed, even as depicted in the Figure 7 and discussed at column 5, lines 54 to 59. A CCD memory device of Trost has the capability of operating in an internal clock sense between minimum and maximum data clock rates. As such, the fact

that Trost also teaches a variable clocking rate for the data transfers between devices 10 and 11 does not belittle the merits of the rejection as applied to the claimed invention.

In the context of asserting that independent claim 1 is patentable because of the language recited in the "at least R buffer registers" clause as quoted at page 14 of the brief, the position advocated is that an optimum number of registers is therefore available for use without any overrun or superfluous number of registers. As pointed out by the examiner at page 11 of the answer, the disclosure is consistent with the argument that a minimum number of registers is determined according to the relationship set forth in the claim and in accordance with the "at least" language of the above-noted clause. Appellants' arguments as to this clause of claim 1 on appeal do not assert that Trost does not teach or suggest to the artisan within 35 U.S.C. § 103 the subject matter of this clause. As noted again by the examiner at page 11 of the answer, the examiner has asserted that there are portions specifically identified in Trost to meet the language of that clause.

As to dependent claims 2 to 5, the positions set forth by appellants at page 15 of the brief indicate that they have not argued the particulars of these respective claims in any manner

but have asserted only a general argument of patentability, which is unacceptable as an argumentative approach within 37 CFR § 1.192.

In a similar manner, the subject matter of independent claims 8 and 9 is considered to be a broader recitation of the subject matter directly corresponding to independent claim 1 on appeal. More specifically, the above-noted "at least R buffer registers" clause of claim 1 on appeal is only recited in these claims 8 and 9 as "for receiving data from the first device, R being an integer number greater than 1." Similarly, the counting means clause of independent claim 1 is only recited in independent claims 8 and 9 as "generating a predetermined number of distinct values in response to the strobe signals applied thereto." In accordance with the examiner's reasoning, these claims are broader than the corresponding recitation in independent claim 1 on appeal. Therefore, the teachings as correlated by the examiner to claim 1 obviously would have been even more applicable to the artisan to claims 8 and 9.

We part company with the examiner's rejection of dependent claims 6 and 7 on appeal within 35 U.S.C. § 103 in light of the collective teachings of Trost and Meinke. Assuming for the sake of argument that it would have been proper within this statutory

provision for the artisan to have combined the teachings of these two references, the subject matter of these two dependent claims 6 and 7 would not have been met. The respective overrun detection means and validation means in these claims 6 and 7 require specific relationships between the latches in these claims to other circuit elements, none of which has been detailed by the examiner as being correlated to any of the collective teachings and suggestions between the two references. As such, the examiner has failed to set forth a prima facie case of obvious-ness of the specific subject matter set forth in these two claims even though the examiner appears to have set forth a valid basis between the two references only for the concept of both claims, that is, the overrun detection concept, as well as the validation concept set forth in respective claims 6 and 7.

In view of the foregoing, the decision of the examiner is affirmed as to the decision to reject claims 1 to 5, 8 and 9 within 35 U.S.C. § 103, but is reversed as to the examiner's decision to reject dependent claims 6 and 7 under this statutory provision. Therefore, the decision of the examiner is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

James D. Thomas Administrative Patent Judge	)
John C. Martin Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
Jameson Lee Administrative Patent Judge	)

Appeal No. 96-0033
Application 08/066,638

Joscelyn C. Cockburn
972/B205, IBM Corporation
P. O. Box 12195
Research Triangle Park, NC 27709

JDT/cam